What is claimed is:

1. A method for forming plugs on active regions of a semiconductor device, comprising the steps of:

forming a plurality of gate lines on a substrate;

forming a plurality of cell junctions by ion-implanting a first dopant with use of the gate lines as a mask;

forming a buffer layer along a gate line profile; and

forming a plurality of plug ion-implantation regions in the cell junctions by ion-implanting a second dopant into the substrate under the presence of the buffer layer to thereby from the plugs thereon.

2. The method as recited in claim 1, wherein the plug ion-implantation region is formed by employing a blanket ion-implantation technique without using a mask.

3. The method as recited in claim 2, wherein the blanket ion-implantation process proceeds by employing phosphorus ^{31}P with a dose ranging from about 1×10^{12} ions/cm^2 to about 3×10^{13} ions/cm^2 and an implantation energy ranging from about 80 keV to about 150 keV.

4. The method as recited in claim 2, wherein the blanket ion-implantation process proceeds by employing ^{31}P with distributed energy within a range from about 80 keV to

about 150 keV and dose within a range from about 1×10^{12} ions/cm^2 to about 3×10^{13} ions/cm^2 both being applied in several sets.

5. The method as recited in claim 4, wherein the blanket ion-implantation process with distributed energy is carried out in several sets by increasing energy from a high level to a low level but within a range from about 80 keV to about 150 keV.

6. The method as recited in claim 1, wherein the buffer layer is a nitride layer.

7. The method as recited in claim 2, wherein the nitride layer has a thickness in a range from about 200 Å to about 500 Å.

8. The method as recited in claim 1, wherein the first dopant and the second dopant are N-type dopants.

9. The method as recited in claim 1, further comprising the steps of:

forming a spacer at both sidewalls of each gate line by etching the buffer layer;

forming an inter-layer insulation layer on a resultant substrate structure;

forming a plurality of contact holes exposing a

surface of each cell junction by etching the inter-layer insulation layer; and

forming a plurality of contact plugs electrically connected to the cell junctions through the contact holes.

10. A method for fabricating a semiconductor device, comprising the steps of:

forming a plurality of gate lines on a substrate;

forming a plurality of cell junctions by ion-implanting a first dopant with use of the gate lines as a mask;

forming a buffer layer along a gate line profile; and

forming a plurality of plug ion-implantation regions in the cell junctions by ion-implanting a second dopant into the substrate under the presence of the buffer layer.

11. The method as recited in claim 10, wherein the plug ion-implantation region is formed by employing a blanket ion-implantation technique without using a mask.

12. The method as recited in claim 11, wherein the blanket ion-implantation process proceeds by employing phosphorus ^{31}P with a dose ranging from about 1×10^{12} ions/cm^2 to about 3×10^{13} ions/cm^2 and an implantation energy ranging from about 80 keV to about 150 keV.

13. The method as recited in claim 11, wherein the

blanket ion-implantation process proceeds by employing ^{31}P with distributed energy within a range from about 80 keV to about 150 keV and dose within a range from about 1×10^{12} ions/cm^2 to about 3×10^{13} ions/cm^2 both being applied in several sets.

14. The method as recited in claim 13, wherein the blanket ion-implantation process with distributed energy is carried out in several sets by increasing energy from a high level to a low level but within a range from about 80 keV to about 150 keV.

15. The method as recited in claim 10, wherein the buffer layer is a nitride layer.

16. The method as recited in claim 11, wherein the nitride layer has a thickness in a range from about 200 Å to about 500 Å.

17. The method as recited in claim 10, wherein the first dopant and the second dopant are N-type dopants.

18. The method as recited in claim 10, further comprising the steps of:

forming a spacer at both sidewalls of each gate line by etching the buffer layer;

forming an inter-layer insulation layer on a resultant

substrate structure;

forming a plurality of contact holes exposing a surface of each cell junction by etching the inter-layer insulation layer; and

forming a plurality of contact plugs electrically connected to the cell junctions through the contact holes.